invention. This operation is intended to correct those over erase cells in the erased block. Any cells with Vt below Vt-1 (67) have to be corrected to have a Vt, which is above Vt-1 using correction 68 which increases the Vt of a cell. The page verification is continued until all pages 69 and 70 in a block have been corrected. With the three concurrent applied word line voltages, Vcorrection for page correction 68 and Vcorvfy for page correction verification 67 this operation can be performed on a bit-by-bit basis. The operation will stop when all pages have been corrected.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method to provide storage operations for an ETOX NOR memory array on a P-substrate using three concurrent word line voltages, comprising:

a) applying a first voltage to a selected word line in a selected memory block of an ETOX NOR memory array to control a memory operation,

b) applying a second voltage to a non-selected word line in said selected memory block to eliminate bit line leakage in the selected memory block.

c) applying a third voltage to said non-selected word line in non-selected blocks of said memory array to prevent disturb conditions,

d) continuing the application of the three word line voltages until all word lines is said selected block have been processed.

2. The method in claim 1, wherein said memory operation is block erase verify.

3. The method in claim 1, wherein said memory operation is cell voltage correction.

4. The method in claim 1, wherein said memory operation is cell voltage correction verify.

5. A method to provide storage operations for an AND memory array on a P-substrate using three concurrent word line voltages, comprising:

a) applying a first voltage to a selected word line in a selected memory block of an AND memory array to control a memory operation,

b) applying a second voltage to a non-selected word line in said selected memory block to eliminate bit line leakage in the selected memory block.

c) applying a third voltage to said non-selected word line in non-selected blocks of said memory array to prevent disturb conditions,

d) continuing the application of the three word line voltages until all word lines is said selected block have been processed.

6. The method in claim 5, wherein said memory operation is random page erase using edge erase.

7. The method in claim 5, wherein said memory operation is block erase verify.

8. The method in claim 5, wherein said memory operation is block erase inhibit for an edge erase operation.

9. The method in claim 5, wherein said memory operation is cell voltage correction.

10. The method in claim 5, wherein said memory operation is cell voltage correction verify.

11. The method in claim 5, wherein said memory operation is random page program.

12. A method to provide storage operations for an ETOX NOR memory array on a P-well using three concurrent word line voltages, comprising:

a) applying a first voltage to a selected word line in a selected memory block of an AND memory array to control a memory operation,

b) applying a second voltage to a non-selected word line in said selected memory block to eliminate bit line leakage in the selected memory block.

c) applying a third voltage to said non-selected word line in non-selected blocks of said memory array to prevent disturb conditions,

d) continuing the application of the three word line voltages until all word lines is said selected block have been processed.

13. The method in claim 12, wherein said memory operation is block erase verify.

14. The method in claim 12, wherein said memory operation is cell voltage correction.

15. The method in claim 12, wherein said memory operation is cell voltage correction verify.

16. A method for erasing a block of a flash memory array using three consecutive bias conditions, comprising:

a) applying a first set of bias conditions to a block of cells of a flash EEPROM memory array to erase said block of cells,

b) applying a second set of bias conditions to a page of cells of said block of cells to verify that cells in said page have a Vt (threshold voltage) less than a predetermined value,

c) applying a third set of bias conditions to inhibit from further erasure said page of cells that are verified to be erased,

d) continuing until all cells in said block are erased and verified to be erased.

17. The method of claim 16, wherein applying said first set of bias conditions includes a large magnitude negative voltage applied to a word line to erase floating gates of said block of cells.

18. The method of claim 16, wherein applying said second set of bias conditions includes a voltage applied to a word line to verify the Vt of said page of cells is less than said predetermined value.

19. The method of claim 16, wherein applying said third set of bias conditions includes a voltage applied to a word line to inhibit cells on said word line from further erasure.

20. The method of claim 16, wherein said flash EEPROM memory array is an ETOX NOR type memory array.

21. The method of claim 20, wherein applying the second set of bias conditions causes a FN (Fowler-Nordheim) channel erase operation, or a FN edge erase operation.

22. The method of claim 16, wherein said flash EEPROM memory array is a NOR type AND memory array.

23. The method of claim 22, wherein applying the second set of bias conditions causes a FN channel erase operation.

24. The method of claim 16, wherein blocks not being erased are biased to prevent an erase disturb.

25. A method for erasing cells in a flash memory array, comprising:

a) a means for selecting cells of a flash EEPROM array to be erased,

b) a means for reducing Vt (cell threshold voltage) below a first predetermined value.

c) a means for verifying said Vt is below said first predetermined value,

d) a means for detecting said Vt is below a second predetermined value which is less positive than said first predetermined value,

e) a means for increasing said Vt to a value above said second predetermined value and below said first predetermined value,

f) a means for verifying said Vt is a value between said first and said second predetermined values.

26. The method of claim 25, wherein said flash EEPROM array is an ETOX NOR type non-volatile memory array.

27. The method of claim 25, wherein said flash EEPROM array is an AND type non-volatile memory array.